

Programming Models and Development Software for a Space-Based Many-Core Processor

Stephen P. Crago, Dong-In Kang, Mikyung Kang, Robert Kost, Karandeep Singh, Joseph Suh, John Paul Walters,

University of Southern California / Information Sciences Institute
Arlington, Virginia, USA
crago@isi.edu

Abstract—The Maestro processor is a 49-core many-core processor for space based on the TILE64 architecture and implemented in rad-hard-by-design technology by Boeing. In this paper we discuss the programming models for Maestro, the implications of the programming model on fault tolerance and flight software, and the software development tools that have been developed for Maestro. The software

Multi-core programming; space-based processing; parallel software.

Described here is experimental development software that allows application and algorithm evaluation on the architecture, but we believe this software can be used as the basis for flight software. The software includes libraries, performance analysis and optimization tools, and compilers. While this work was done on the Maestro chip, the principles discussed can be applied to any multi-core or many-core processor.