

# Porting the Cosmic-Ray Rejection Application CRBLASTER to an Early MAESTRO Development Board

Kenneth Mighell  
National Optical Astronomy Observatory

*Abstract*—I will discuss my experience of porting a NASA-funded parallel-processing cosmic-ray rejection application, called CRBLASTER, to the new 49-core RHDB (Radiation Hardened By Design) MAESTRO processor on an early MAESTRO Development Board (MDB) with a 350 MHz Interim Test Chip (ITC). The MDB used for this port is located at ISI East which is the Arlington, Virginia unit of the Information Sciences Institute of the University of California. The total time to port CRBLASTER from a 64-core Tiler TILE64 processor on a TILExpress-64 card to the 49-core MAESTRO processor on the MAESTRO Development Board was about

20 hours spread over a few days. Running CRBLASTER on a 100 MHz ITC revealed the need to optimize memory access procedures which were implemented in a revised MDB with a 350 MHz ITC. CRBLASTER scales well on the early MDB but not as well as on the TILExpress-64 card. It is still early days for the MAESTRO processor and MAESTRO development boards. These early results indicate that the MAESTRO processor has great potential to become a powerful enabling technology for the next generation of U.S. satellites and NASA astrophysical missions.